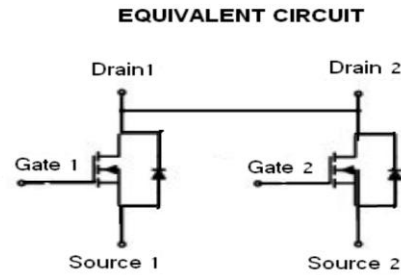
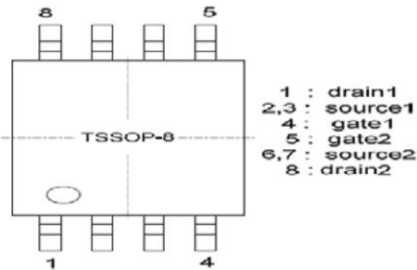




8205A 20V N-Channel MOSFET

General Description

The 8205A is a dual N-channel MOS Field Effect Transistor which uses advanced trench technology to provide excellent $R_{DS(on)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch.



Featuration

- $V_{DS(max)} = 20V$;
- $I_{D(max)} = 6.0A$;
- Low on-state resistance
 - $R_{DS(on)} = 23m\Omega$ TYP. ($V_{GS} = 4.5V$)
 - $R_{DS(on)} = 24m\Omega$ TYP. ($V_{GS} = 3.8V$)
 - $R_{DS(on)} = 27m\Omega$ TYP. ($V_{GS} = 2.5V$)
- Lead free product is acquired;
- Surface Mount Package;

Applications

- Battery protection.
- Battery Powered Systems.
- Power Management in Notebook Computer
- Portable Equipment

Maximum Ratings ($T_a = 25^\circ C$)

Parameter	Symbol	Value	Units
Drain to Source Voltage	VDSS	20	V
Gate to Source Voltage	VGSS	± 12	V
Continuous Drain Current	25°C	ID	6.0
	85°C		4.8
Pulsed Drain Current	ID(pulse)	24	A
Maximum Power Dissipation	25°C	PD	1.25
Operating Junction Temperature	TJ	+150	°C
Storage Temperature	TSTG	-55--+150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	TL	260	°C



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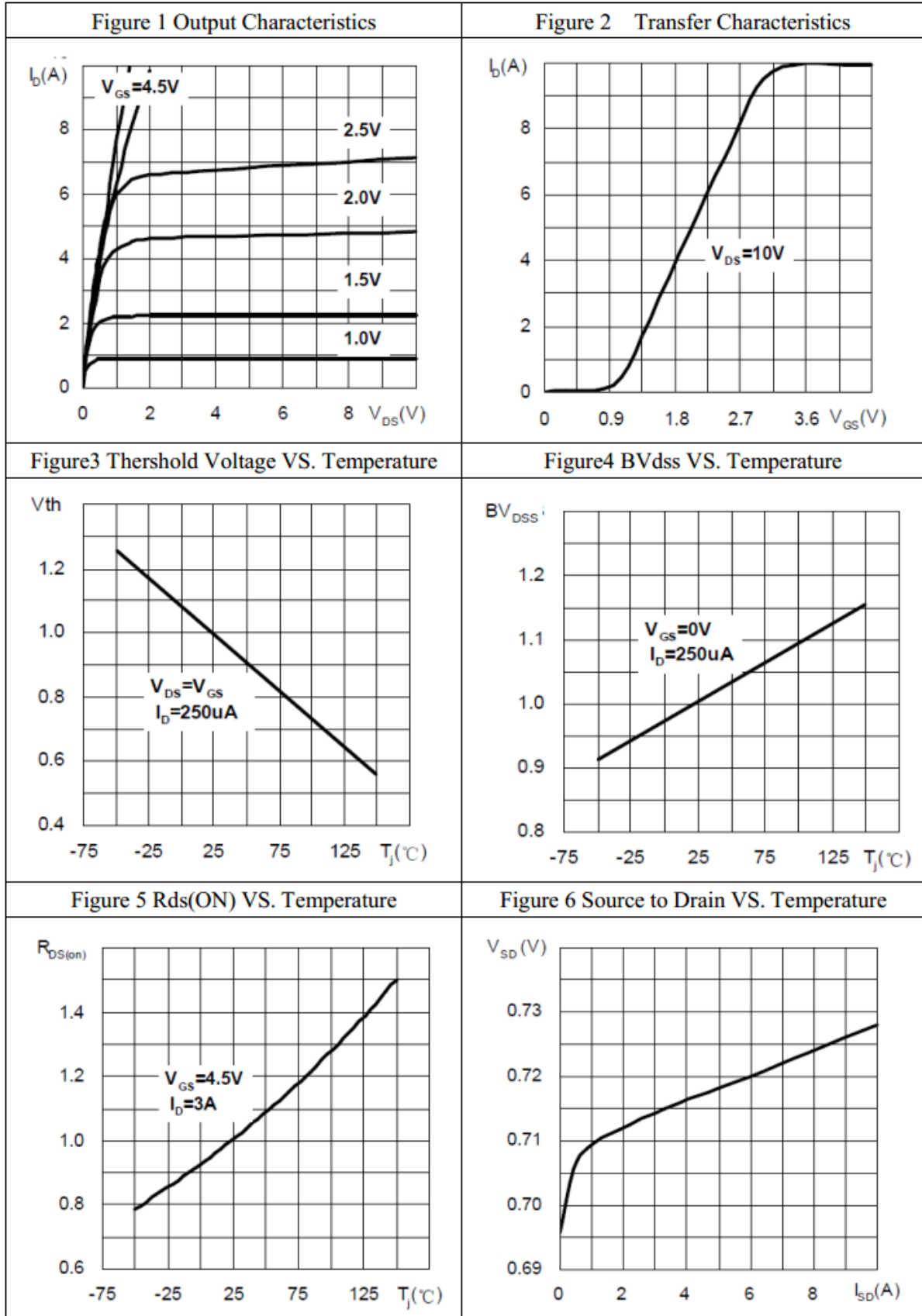
TEL: 0755-23077644 / 0755-27805705

Electrical Characteristics (TA = 25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Units
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _{DS} =250uA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} =0V			1	uA
Gate Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V			±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = 250μA	0.55	0.85	1.15	V
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 4.5V, I _D =3.0A		23	25	mΩ
		V _{GS} = 3.8V, I _D =3.0A		24	26	mΩ
		V _{GS} = 2.5V, I _D =2.0A		27	35	mΩ
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =10V, f=1.0MHZ		370		pF
Output Capacitance	C _{oss}			89		pF
Reverse Transfer Capacitance	C _{rss}			10		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _{DS} =3.0A, V _{GS} =4.5V, R _G =10Ω		200		nS
Rise Time	t _r			236		nS
Turn-off Delay Time	t _{d(off)}			36		nS
Fall Time	t _f			165		nS
Total Gate Charge	Q _G	V _{DD} =10V, I _D =1.0A, V _{GS} =4.5V,		7.5		nC
Gate to Source Charge	Q _{GS}			3.0		nC
Gate to Drain Charge	Q _{GD}			1.5		nC
Drain-Source Diode Forward Voltage	V _{SD}	I _S =2.8A, V _{GS} =0V		0.7	1.3	V



Typical characteristics (25°C unless noted)





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Figure 7 Capacitance

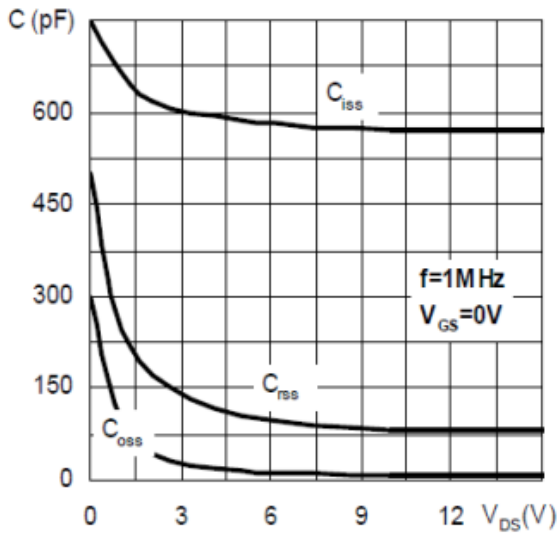


Figure 8 Gate Charge

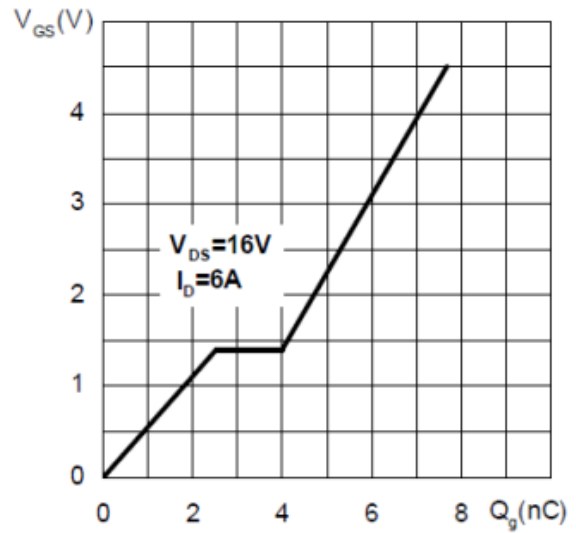


Figure 9 Safe Operating Area

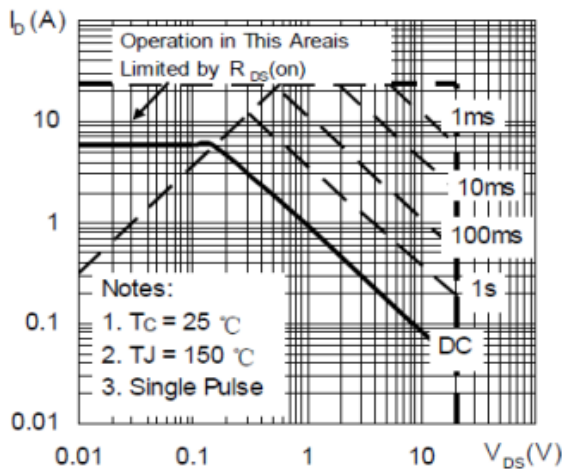


Figure 10 Maximum Drain Current VS. Case Temperature

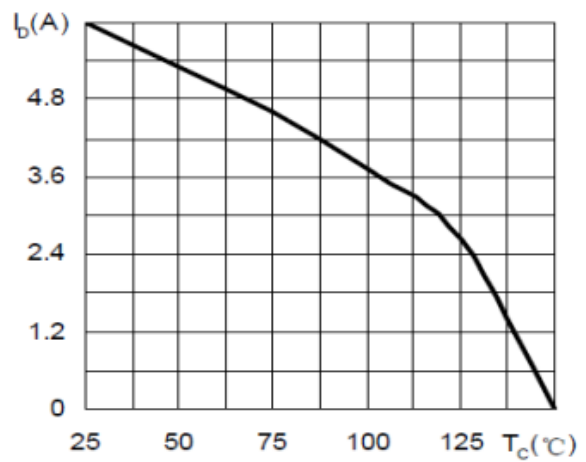
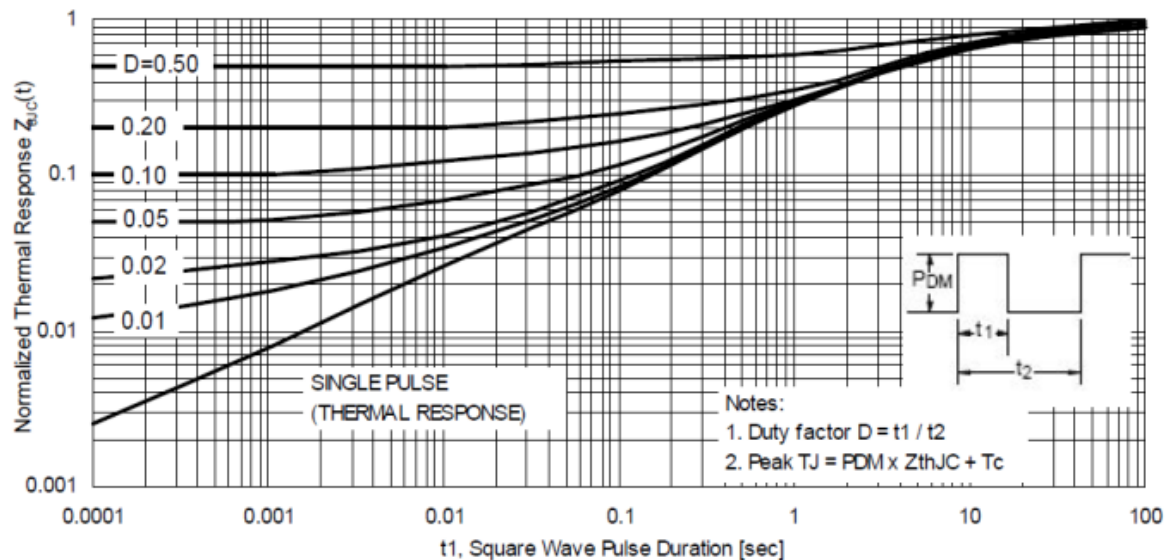


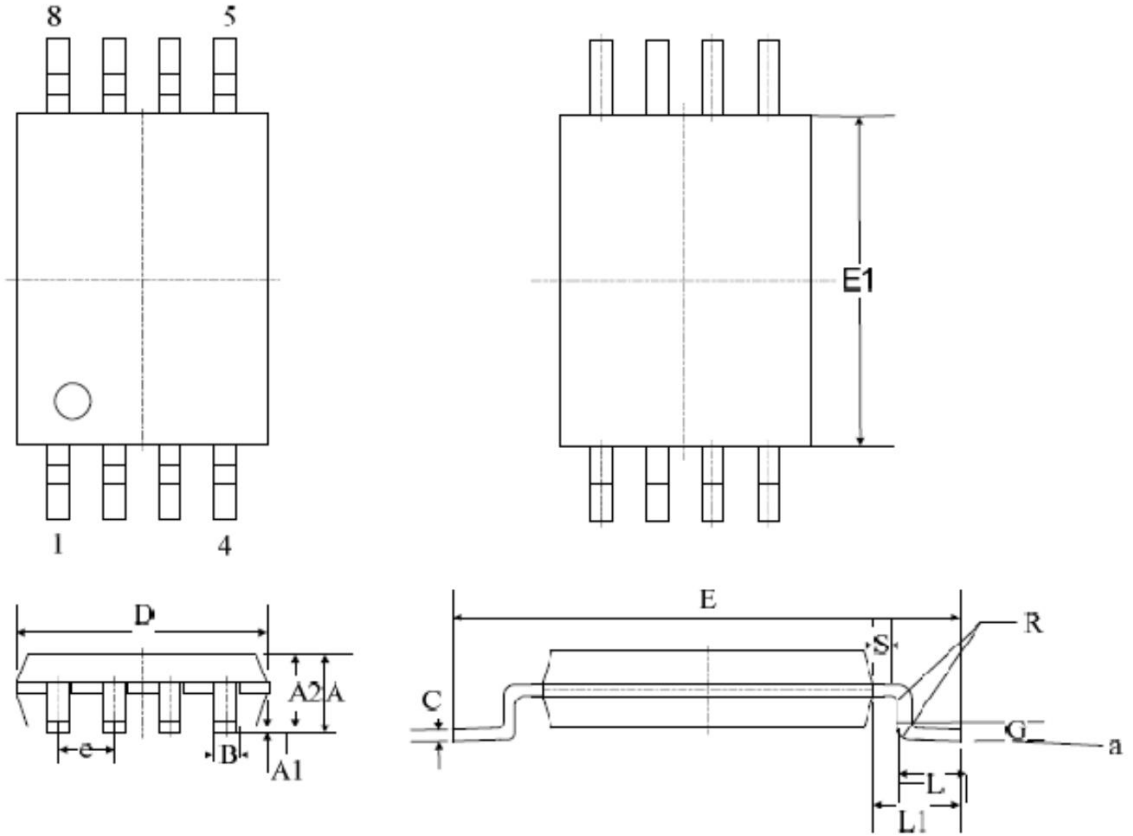
Figure 10 Maximum Transient Thermal Impedence





Package Dimensions:

TSSOP-8



Dimensions (unit: mm)

DIM		A	A(1)	A(2)	B	C	D	E	E1	e	G	L	L1	a	R	S		
MM	Min.	1.05	0.05	0.99	0.19		2.9	6.2	4.3	0.65 BSC	0.254 GAGE PLANE	0.45	0.9	0°	0.09	0.2		
	Nom.	1.1	0.1	1.02	0.25	0.127	3	6.4	4.4			0.6	1	4°				
	Max.	1.2	0.15	1.05	0.3		3.2	6.6	4.5			0.75	1.1	8°				